Fabio Frustaci – Professional CV

General Information

Place of birth:	Reggio Calabria (ITALY)
Date of birth:	January, 13th 1979
Nationality:	Italian
Education:	PhD in Electronics Engineering
Position:	Associate Professor, Department DIMES, University of Calabria, Italy
Office:	+39 0984 494108
Email:	f.frustaci@dimes.unical.it
Researchgate:	https://www.researchgate.net/profile/Fabio_Frustaci
Scopus:	https://www.scopus.com/authid/detail.uri?authorId=14631848300
Google Scholar:	https://scholar.google.it/citations?user=cOMXOyUAAAAJ&hl=it

Education:

University “Mediterranea” of Reggio Calabria, Italy:

November 2003 - March 2007	**PhD in Electronics Engineering**. Thesis title "Low-power SRAM cache memories design". Supervisor*:* Prof. Pasquale Corsonello.
Sept 1997 - May 2003	5 years laurea degree (equivalent to a bachelor + a master) in Electronics Engineering (110/110 cum laude). Thesis title: “Optimum sizing criteria for CMOS digital adders”

Professional experiences:

Jan. 2023: National Scientific Qualification for the role of Full Professor in the SSD ING/INF 01

Aug. 2021 – today: Associate Professor in Electronics, Dept. DIMES University of Calabria.

Dec. 2014 – July 2021: Assistant Professor in Electronics, Dept. DIMES University of Calabria.

Aug. 2011 – August 2014 Visiting Researcher at the Dept. EECS, University of Michigan, Ann Arbor, MI, USA.

Jan. 2007 – Nov. 2014: Research Fellow in Electronics, Dept. DIMES University of Calabria.

June 2006-Oct. 2006: Visiting Scholar at the Dept. ECE, University of Rochester, Rochester (NY), USA.

Main research topics:

- Modelling of sub-threshold CMOS circuits.

- Ultra low-power VLSI design (both SRAM memory and arithmetic circuits).

- Design of VLSI circuits with high noise robustness and high yield.

- Emerging technologies (quantum-dot cellular automata, Ferroelectric CMOS).

- Approximate Computing.

- Hardware/Software co-design on FPGA-based heterogeneous SoCs.

- Low-power embedded system for Artificial Intelligence - and Machine Learning-based applications.

Teaching experience:

Lecturer:

Academic years 2022-2023-2024

"*Approximate Computing & Digital Systems*" Ph.D. course in IoT, Dept. DIMES, Università della Calabria, Italy

Academic years 2023-2024

"*High Level Synthesis of Digital Systems* " (6 CFU), Master Degree in Electronics Engineering, Dept. DIMES, Università della Calabria, Italy

Academic years 2023-2024

"*Microcontroller Lab*" (6 CFU), Bachelor Degree in Electronics Engineering, Dept. DIMES, Università della Calabria, Italy

Academic years 2021-2022

"*Electronics for IoT Devices*" (6 CFU), Master Degree in Computer Science, Dept. DIMES, Università della Calabria, Italy

Academic years 2016-2017-2018-2019-2020-2021-2022-2023-2024

"*Low-Power Design*" (6 CFU), Master Degree in Electronics Engineering, Dept. DIMES, Università della Calabria, Italy

Academic years 2008-2009-2010

"*Analogue Electronics*" Master Degree in Mechanical Engineering, Dept. DIMES, Università della Calabria, Italy

Assistant Lecturer (responsible for the lab teaching):

Academic years 2015-2016-2017-2018-2019-2020-2021-2022

"*FPGA Architecture and Design*" Bachelor Degree in Electronics Engineering, Dept. DIMES, Università della Calabria, Italy

Academic years 2015-2016-2017

"*Digital Electronics*" Master Degree in Electronics Engineering, Dept. DIMES, Università della Calabria, Italy

Academic years 2007-2008-2009-2010-2011-2012

"*Analogue Electronics*" Master Degree in Mechanical Engineering, Dept. DIMES, Università della Calabria, Italy

Academic years 2005-2006-2010-2011

"*VLSI design*" Bachelor Degree in Electronics Engineering, Dept. DIMES, Università della Calabria, Italy

Thesis supervisor:

2013-2024: Supervisor of ten Master students for the fulfilment of the Master Degree in Electronics Engineering, Università della Calabria, Italy.

PhD committee member:

Academic years 2015-2024

Member of the PhD committee of the PhD program "Information and Communication Technology (ICT), Università della Calabria, Italy

Speaker at international conferences:

May 2006: IEEE International Symposium on Circuits and Systems (ISCAS 2006), May 21-24 2006, Kos Island, Greece.

June 2006: The 2nd IEEE Conference on Ph.D. Research in MicroElectronics and Electronics (PRIME 2006), June 12-15 2006, Otranto, Italy.

July 2007: The 3rd Conference on Ph.D. Research in MicroElectronics and Electronics (PRIME 2007), July 2-5 2007, Bordeaux; France.

Sept. 2008: 18th International Workshop on Power and Timing Modeling, Optimization and Simulation, (PATMOS 2008), September 10-12 2008, Lisboa, Portugal.

Sept. 2009: 19th International Workshop on Power and Timing Modeling, Optimization and Simulation, (PATMOS 2009), September 9-11 2009, Delft, The Netherlands

April 2010: SPIE - The International Society for Optical Engineering (VLSI Circuits and Systems V), 18-20 April 2010, Prague, Czech Republic

May 2010: IEEE International Symposium on Circuits and Systems: Nano-Bio Circuit Fabrics and Systems (ISCAS 2010), May 30-June 2 2010, Paris, France

Dec. 2010: International Conference on Microelectronics, ICM 2010, December 19-22 2010 Il Cairo, Egypt.

Oct. 2015: The 33rd IEEE International Conference on Computer Design (ICCD 2015), October 18-21 2015, New York, USA

Oct. 2019: The IEEE International Conference on Circuits and Systems (ISCAS 2019), June 2019, Sapporo, Japan

Sept. 2022: The International Conference on Applied Intelligence and Informatics (AII 2022), Sept. 2022, Reggio Calabria, Italy.

Responsibility in research projects:

2006-2007: Principal investigator for the project for the project "Low-power and high-speed SRAM memories in sub-micrometer technologies" (4,500 EURO). Granted by the University of Calabria.

2011-2014: Principal investigator for the project "Innovative schemes for ultra-low power SRAMs with ultra-low leakage and improved robustness for biomedical and green

electronics". Granted by: Fondo Sociale Europeo (FSE), Programma Operativo Regionale (POR) Calabria FSE 2007/2013, Italian Government (64,000 EURO).

2018-2021: Responsable of the local unity of the University of Calabria within the work package 3.1 of the project “Design of intelligent sensors for components monitoring and data acquisition” Granted by Minister of Education, University and Research, Italian Government. CodeARS01_01061. (PI: “Centro Ricerche FIAT”- CRF- Stellantis group. Total amount of the funding: 9,947,838.33 EURO).

2023- Participation to the research activities of the PRIN 2022 2022T2XNJE “A framework for COntinuum COmputing WEARable Systems (COCOWEARS)” - CUP: H53D23003640006 – Research unit of the University of Calabria - DIMES

Other Professional Activities:

2016 – today: Editor of the journal “Microelectronics Journal”

2008- today: Peer Reviewer:for the following international journals:

- IEEE Transactions on VLSI
- IEEE Transactions on Circ. and Syst. I- Regular Papers
- IEEE Transactions on Circ. and Syst. II- Express Brief
- IEEE Transactions on Nanotechnology
- IEEE Journal on Emerging and Selected Topics in Circuits and Systems
- Microelectronics Journal
- Integration, the VSLI Journal
- Journal of Low Power Electronics
- Journal of Circuits, Systems and Computers
- Sensors

2010 – today:
Partecipation as TPC member for the following international conferences:

ICETET2019, ICCD2010, ICCD2011, ICCD2012, ICCD2013, NEWCAS2015, ICCD2016, ICCD2018, ICCD2019, NEWCAS 2022, AII2022.

Publications:

Journal:

[1]. Ieracitano C., Mammone N., Spagnolo F., **Frustaci F**., Perri S., Corsonello P., Morabito F. C. (2024). An explainable embedded neural system for on-board ship detection from optical satellite imagery. ENGINEERING APPLICATIONS OF ARTIFICIAL INTELLIGENCE, vol. 133, ISSN: 0952-1976, doi: 10.1016/j.engappai.2024.108517

[2]. Spagnolo F., Corsonello P., **Frustaci F**., Perri S (2024). Approximate bilateral filters for real-time and low-energy imaging applications on FPGAs. THE JOURNAL OF SUPERCOMPUTING, ISSN: 0920-8542, doi: 10.1007/s11227-024-06084-y

[3]. Spagnolo, Fanny, Corsonello, Pasquale, **Frustaci, Fabio**, Perri, Stefania (2024). Efficient Addition Circuits Using Three-Gate Reconfigurable Field Effect Transistors. JOURNAL OF

LOW POWER ELECTRONICS AND APPLICATIONS, vol. 14, p. 1-8, ISSN: 2079-9268, doi: 10.3390/jlpea14020024

[4]. Spagnolo, Fanny, Corsonello, Pasquale, **Frustaci, Fabio**, Perri, Stefania (2024). Efficient implementation of signed multipliers on FPGAs. COMPUTERS & ELECTRICAL ENGINEERING, vol. 116, p. 1-11, ISSN: 0045-7906, doi: 10.1016/j.compeleceng.2024.109217

[5]. Fanny Spagnolo, Stefania Perri, Massimo Vatalaro, **Fabio Frustaci**, Felice Crupi, Pasquale Corsonello (2024). Exploring the Usage of Fast Carry Chains to Implement Multistage Ring Oscillators on FPGAs: Design and Characterization. IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, p. 1-13, ISSN: 1063-8210, doi: 10.1109/TVLSI.2024.3395302

[6]. Spagnolo F., Corsonello P., **Frustaci F**., Perri S. (2023). Design of Approximate Bilateral Filters for Image Denoising on FPGAs. IEEE ACCESS, vol. 11, p. 1990-2000, ISSN: 2169-3536, doi: 10.1109/ACCESS.2022.3233921

[7]. Perri, Stefania, Spagnolo, Fanny, **Frustaci, Fabio**, Corsonello, Pasquale (2023). Design of Leading Zero Counters on FPGAs. IEEE EMBEDDED SYSTEMS LETTERS, vol. 15, p. 149-152, ISSN: 1943-0663, doi: 10.1109/LES.2022.3217861

[8]. Spagnolo F., Corsonello P., **Frustaci F**., Perri S. (2023). Design of a Low-Power Super-Resolution Architecture for Virtual Reality Wearable Devices. IEEE SENSORS JOURNAL, vol. 23, p. 9009-9016, ISSN: 1530-437X, doi: 10.1109/JSEN.2023.3256524

[9]. Abhilasha Dave, **Fabio Frustaci**, Fanny Spagnolo, Mikail Yayla, Jian-Jia Chen, Hussam Amrouch (2023). HW/SW Codesign for Approximation-Aware Binary Neural Networks. IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS, vol. 13, p. 33-47, ISSN: 2156-3357, doi: 10.1109/JETCAS.2023.3243267

[10]. Yayla, Mikail, **Frustaci, Fabio**, Spagnolo, Fanny, Chen, Jian-Jia, Amrouch, Hussam (2023). Unlocking Efficiency in BNNs: Global by Local Thresholding for Analog-based HW Accelerators. IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS, p. 1, ISSN: 2156-3357, doi: 10.1109/JETCAS.2023.3315561

[11]. Perri S., Spagnolo F., **Frustaci F**., Corsonello P. (2023). Welding defects classification through a Convolutional Neural Network. MANUFACTURING LETTERS, vol. 35, p. 29-32, ISSN: 2213-8463, doi: 10.1016/j.mfglet.2022.11.006

[12]. **Frustaci, Fabio**, Spagnolo, Fanny, Perri, Stefania, Corsonello, Pasquale (2022). A High-Speed FPGA-based True Random Number Generator using Metastability with Clock Managers. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS. II, EXPRESS BRIEFS, vol. 70, p. 756-760, ISSN: 1549-7747, doi: 10.1109/TCSII.2022.3211278

[13]. Perri, Stefania, Spagnolo, Fanny, **Frustaci, Fabio**, Corsonello, Pasquale (2022). Designing Energy-Efficient Approximate Multipliers. JOURNAL OF LOW POWER ELECTRONICS AND APPLICATIONS, vol. 12.

[14]. Perri S., Spagnolo F., **Frustaci F**., Corsonello P. (2022). Multi-Bit Full Comparator Logic in Quantum-Dot Cellular Automata. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS. II, EXPRESS BRIEFS, vol. 69, p. 4508-4512,

[15]. **F. Frustaci**, F. Spagnolo, S. Perri, G. Cocorullo, P. Corsonello, “Robust and High-Performance Machine Vision System for Automatic Quality Inspection in Assembly Processes,” Sensors, vol. 22 (8) pp. 2839-2854, 2022.

[16]. S. Perri, F. Spagnolo, **F. Frustaci**, P. Corsonello “Accuracy Improved Low-Energy Multi-Bit Approximate Adders in QCA”, IEEE Transactions on Circuits and Systems II: Express Briefs 68 (11), 3456-3460, 2021.

[17]. **F. Frustaci**, “Improving the Quality Degradation of Dynamically Configurable Approximate Multipliers via Data Correlation”, Electronics, vol 10 (17), 2021.
[18]. **F Frustaci**, S Perri, P Corsonello, M Alioto “Approximate multipliers with dynamic truncation for energy reduction via graceful quality degradation” IEEE Transactions on Circuits and Systems II: Express Briefs 67 (12), 3427-3431, 2021.
[19]. **F Frustaci**, S Perri, G Cocorullo, P Corsonello, “An embedded machine vision system for an in-line quality check of assembly processes”, Procedia Manufacturing 42, 211-218, 2020.
[20]. S. Perri, F. Spagnolo, **F. Frustaci**, P. Corsonello “Efficient approximate adders for FPGA-based data-paths”, Electronics, vol. 9 (9), 2020.
[21]. F. Spagnolo, S. Perri, **F. Frustaci**, P. Corsonello “Energy-efficient architecture for CNNs inference on heterogeneous FPGA” Journal of Low Power Electronics and Applications, vol. 10, 2020.
[22]. S. Perri, **F. Frustaci**, F. Spagnolo, P. Corsonello, “Stereo Vision Architecture for Heterogeneous Systems-on-Chip, the Journal of Real-Time Image Processing, 17 (2), 393-415, 2020.
[23]. **F Frustaci**, S Perri, P Corsonello, M Alioto “Energy-quality scalable adders based on nonzeroing bit truncation”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems 27 (4), 964-968, 2019.
[24]. F. Spagnolo, **F. Frustaci**, S. Perri, P. Corsonello, “An Efficient Connected Component Labeling Architecture for Embedded Systems”, Journal of Low Power Electronics and Applications, 8(1), pp. 1-11, 2018.
[25]. G. Cocorullo, P. Corsonello, **F. Frustaci**, S. Perri, “Design of Efficient BCD Adders in Quantum-Dot Cellular Automata”, IEEE Transactions on Circuits and Systems II: Express Briefs, 64 (5), pp. 575-579, 2017.
[26]. G. Cocorullo, P. Corsonello, **F. Frustaci**, S. Perri, “An efficient hardware-oriented stereo matching algorithm”, Microprocessors and Microsystem, 46, pp. 21-33, 2016.
[27]. **F. Frustaci**, D. Blaauw, D. Sylvester, M. Alioto “Approximate SRAMs with dynamic energy-quality management”, IEEE Transactions on VLSI Systems, 24 (6), 2128-2141, 2016.
[28]. G Cocorullo, P Corsonello, **F Frustaci**, S Perri, “Design of efficient QCA multiplexers”, International Journal of Circuit Theory and Applications, vol. 44, n°3, pp. 602-615, 2016.
[29]. G. Cocorullo, P. Corsonello, **F. Frustaci**, Lorena-de-los-Angeles Guachi-Guachi, S. Perri, “Multimodal background subtraction for high-performance embedded systems”, Journal of Real-Time Image Processing, pp. 1-17, 2016.
[30]. P. Corsonello, **F. Frustaci**, S. Perri “Power supply noise in accurate delay model for the sub-threshold domain” Integration, the VLSI Journal, vol. 50, pp. 127-136, 2015
[31]. **Frustaci, F**., Khayatzadeh, M., Blaauw, D., Sylvester, D., Alioto, M. " SRAM for Error-Tolerant Applications With Dynamic Energy-Quality Management in 28 nm CMOS" IEEE Journal of Solid-State Circuits, 50 (5), 1310-1323, 2015.
[32]. P. Corsonello, **F. Frustaci**, S. Perri " Low-Leakage SRAM Wordline Drivers for the 28-nm UTBB FDSOI Technology" IEEE Transactions on VLSI Systems, 23 (12), 3133-3137, 2015.
[33]. Corsonello, P. ; **Frustaci, F**. ; Lanuzza, M. ; Perri, S. "Over/Undershooting Effects in Accurate Buffer Delay Model for Sub-Threshold Domain" IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 61, n° 5, pp. 1456-1464, 2014,

[34]. **Frustaci F**. , Lanuzza M., Perri S., Corsonello P., "Analyzing noise robustness of wide fan-in dynamic logic gates under process variations" International Journal of Circuit Theory and Application, Vol. 42, n°5, pp. 452-467, 2014.

[35]. Raffaele De Rose, Marco Lanuzza, **Fabio Frustaci**, Sohan Purohit " Designing Dynamic Carry Skip Adders: Analysis and Comparison" Circuits, Systems, and Signal Processing, Vol. 33, n° 4, pp.1019-1034, 2014.

[36]. Lanuzza M., De Rose R., **Frustaci F**., Perri S., Corsonello P. "Comparative analysis of yield optimized pulsed flip-flops" Microelectronics Reliability, Vol. 52, n° 8, pp. 1679-1689, 2012.

[37]. **Frustaci F**., Corsonello P. , Perri S. , "Analytical Delay Model Considering Variability Effects in Subthreshold Domain", IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, Vol.59, n.3, pp. 168 - 172.

[38]. Lanuzza M., **Frustaci F**., Perri S., Corsonello P. "Design of Energy Aware Adder Circuits Considering Random Intra-Die Process Variations" Journal of Low Power Electronics and Applications ,2011, Vol. 1, n°1, pp. 97-108.

[39]. **Frustaci F**., Alioto M., Corsonello P. " Tapered-Vth approach for energy-efficient CMOS buffers", IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, Vol. 58 n° 11, pp. 2698-2707

[40]. **Frustaci F**., Perri S, M. Lanuzza, Corsonello P., "Energy-Efficient Single Clock Cycle Binary Comparator". International Journal of Circuit Theory and Applications, 2012, vol. 40, n°3, pp. 237-246.

[41]. Lanuzza M. , Zicari P. , **Frustaci F**. , Perri S. , Corsonello P. , "Exploiting Self-Reconfiguration Capability to Improve SRAM-based FPGA Robustness in Space and Avionics Applications". ACM Transactions on Reconfigurable Technology and Systems, 2010, New Series, vol. 4, n°2, pp. 1-19.

[42]. **Frustaci F**., M. Lanuzza, P. Zicari, Perri S, Corsonello P., "Low-power split-path data driven dynamic logic" IET Circuits, Devices & Systems, 2009, Vol. 3, n. 6, pp. 303-312.

[43]. **Frustaci F**., M. Lanuzza, P. Zicari, Perri S, Corsonello P., "Designing High Speed Adders in Power-Constrained Environments" IEEE Transaction on Circuits and Systems II, 2009, Vol. 56, n.2, pp. 172-176.

[44]. **Frustaci F**., Corsonello P., Perri S., Cocorullo G. "High-performance Noise-tolerant circuit techniques for CMOS dynamic logic" IET Circuits, Devices & Systems, 2008, Vol. 2, n. 6, pp. 537-548.

[45]. **Frustaci F**. , Corsonello P. , Perri S. , Cocorullo G. , " Techniques for Leakage Energy Reduction in Deep Submicron Cache Memories". IEEE Transactions on VLSI Systems, 2006, Vol. 14, n. 11, pp. 1238 – 1249.

Lecture Notes:

[46]. Borelli, Antonio, Spagnolo, Fanny, Gravina, Raffaele, **Frustaci, Fabio** (2022). An FPGA-Based Hardware Accelerator for the k-Nearest Neighbor Algorithm Implementation in Wearable Embedded Systems. In: Mufti Mahmud Cosimo Ieracitano M. Shamim Kaiser Nadia Mammone Francesco Carlo Morabito. Applied Intelligence and Informatics. COMMUNICATIONS IN COMPUTER AND INFORMATION SCIENCE, vol. 1724, p. 44-56, Springer, Cham, ISBN: 978-3-031-24801-6, ISSN: 1865-0929, doi: 10.1007/978-3-031-24801-6_4

[47]. Huzyuk, Roman, Spagnolo, Fanny, **Frustaci, Fabio** (2022). Designing Low-Power and High-Speed FPGA-Based Binary Decision Tree Hardware Accelerators. In: Mufti Mahmud Cosimo Ieracitano M. Shamim Kaiser Nadia Mammone Francesco Carlo

Morabito. Applied Intelligence and Informatics. COMMUNICATIONS IN COMPUTER AND INFORMATION SCIENCE, vol. 1724, p. 57-72, Springer, Cham, ISBN: 978-3-031-24800-9, ISSN: 1865-0929, doi: 10.1007/978-3-031-24801-6_5

[48]. Lanuzza M., De Rose R., **Frustaci F**., Perri S. Corsonello P "Impact of Process Variations on Pulsed Flip-Flops: Yield Improving Circuit-Level Techniques and Comparative Analysis" Proc. PATMOS 10, Grenoble, France, 2010, published in Integrated Circuit and System Design. Power and Timing Modeling, Optimization, and Simulation Lecture Notes in Computer Science Vol. 6448, 2011, pp 180-189.

[49]. Lanuzza M. , Zicari P. , **Frustaci F**. , Perri S. , Corsonello P. , "An Efficient and low-cost design methodology to improve SRAM-based FPGA robustness in space and avionic applications".Proc. ARC 09, 2009 Karlsruhe, Germany, published in Reconfigurable Computing: Architectures, Tools and Applications Lecture Notes in Computer Science Vol. 5453, 2009, pp 74-84.

[50]. **Frustaci F**., Lanuzza M. "A New Optimized High-Speed Low-Power Data-Driven Dynamic (D3L) 32-bit Kogge-Stone Adder". Proc. PATMOS 09, Delft, The Netherlands, 2009, published in Integrated Circuit and System Design, Power and Timing Modeling, Optimization and Simulation, Lecture Notes in Computer Science, Springer-Verlag Berlin Heidelberg 2010, Vol. 5953 pp. 357-366.

[51]. **Frustaci F**. , Corsonello P. , Perri S. , Cocorullo G. , "A New Dynamic Logic Circuit Design for an effective Trade-off between Performance and Energy Dissipation". Proc. of PATMOS 08, Lisbon Portugal, 10-12 Sept., pubblicato in Integrated Circuit and System Design, Power and Timing Modeling, Optimization and Simulation, Lecture Notes in Computer Science, Springer-Verlag Berlin Heidelberg 2009,Vol. 5349 pp. 277-286.

International conferences:

[52]. Spagnolo F., Corsonello P., **Frustaci F**., Perri S. (2024). Approximate Foveated-Based Super Resolution Method for Headset Displays. In: Lecture Notes in Electrical Engineering. LECTURE NOTES IN ELECTRICAL ENGINEERING, vol. 1113, p. 338-344, Springer Science and Business Media Deutschland GmbH, ISBN: 978-3-031-48710-1, ISSN: 1876-1100, ita, 2023, doi: 10.1007/978-3-031-48711-8_40

[53]. Salvatore Scarfone, **Fabio Frustaci**, Stefania Perri, "Design and Analysis of a Leading One Detectorbased Approximate Multiplier on FPGA", SMACD/PRIME 2021; International Conference on SMACD and 16th Conference on PRIME, pp. 1-4, 2021.

[54]. Fanny Spagnolo, **Fabio Frustaci**, Stefania Perri, Pasquale Corsonello, "A High-Performance and Power-Efficient SIMD Convolution Engine for FPGAs", 2020 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS), pp. 1-4, 2020.

[55]. Fanny Spagnolo, Stefania Perri, **Fabio Frustaci**, Pasquale Corsonello, "Reconfigurable convolution architecture for heterogeneous systems-on-chip", 2020 9th Mediterranean Conference on Embedded Computing (MECO), pp. 1-5, 2020.

[56]. Fanny Spagnolo, Stefania Perri, **Fabio Frustaci**, Pasquale Corsonello, "Connected component analysis for traffic sign recognition embedded processing systems", 2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS), pp. 749-752, 2018.

[57]. F Spagnolo, S Perri, **F Frustaci**, P Corsonello, "Designing fast convolutional engines for deep learning applications", 2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS), pp. 753-756, 2018.

[58]. S Perri, F. **Frustaci**, F. Spagnolo, P. Corsonello “Design of Real-Time FPGA-based Embedded System for Stereo Vision”, Proc. of IEEE International Symposium on Circuit and Systems (ISCAS), 2018, Firenze (ITALY), pp. 1-5.

[59]. L. Guachi, G. Cocorullo, P. Corsonello, **F. Frustaci**, S. Perri, “Color Invariant Study for Background Subtraction”, Proc. of the IARIA International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS), 2016, Nice (France), pp. 1-5.

[60]. M. Khayatzadeh, **F. Frustaci**, D. Blaauw, D. Sylvester, M. Alioto “A reconfigurable sense amplifier with 3X offset reduction in 28nm FDSOI CMOS”, IEEE Symposium on VLSI Circuits, Digest of Technical Papers (VLSI), 2015, Kyoto (Japan), pp. 270-271,

[61]. **F. Frustaci**, D. Blaauw, D. Sylvester, M. Alioto, “Better-than-voltage scaling energy reduction in approximate SRAMs via bit dropping and bit reuse”, Proc. of IEEE 25th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), 2015, Bahia (Brazil), pp. 132-139.

[62]. P. Corsonello, **F. Frustaci**, S. Perri, “A layout strategy for low-power voltage level shifters in 28nm UTBB FDSOI technology”, IEEE AEIT International Annual Conference (AEIT), 2015, Naples (Italy), pp. 1-4.

[63]. G. Cocorullo, P. Corsonello, **F. Frustaci**, L. Guachi, S. Perri, “Embedded surveillance system using background subtraction and Raspberry Pi”, IEEE AEIT International Annual Conference (AEIT), 2015, Naples (Italy), pp. 1-4.

[64]. P. Corsonello, S. Perri, **F. Frustaci**, “Exploring well configurations for voltage level converter design in 28 nm UTBB FDSOI technology”, Proc. of IEEE International Conference on Computer Design (ICCD), 2015, New York, USA, pp. 499-504.

[65]. **F. Frustaci**; Khayatzadeh, Mahmood ; Blaauw, David ; Sylvester, Dennis ; Alioto, Massimo "A 32kb SRAM for error-free and error-tolerant applications with dynamic energy-quality management in 28nm CMOS" IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, USA, 2014, pp. 244-245.

[66]. F L. Guachi, G. Cocorullo, P. Corsonello, **F. Frustaci**, S. Perri “A novel background subtraction method based on color invariants and grayscale levels”, Proc. of IEEE International Carnahan Conference on Security Technology (ICCST), 2014, Rome (Italy), pp. 1-5.

[67]. **F. Frustaci**, P Corsonello, M Alioto "Tapered-VTH CMOS buffer design for improved energy efficiency in deep nanometer technology" Proc. of IEEE International Symposium on Circuits and Systems (ISCAS), Rio de Janeiro, Brasile, 2011, 2075-2078.

[68]. S Solanki, **F Frustaci**, P Corsonello " VLSI design of low-leakage single-ended 6T SRAM cell" SPIE Microtechnologies, 2011, Prague (Czech Repubblic), pp 1-4.

[69]. **F. Frustaci**, P Corsonello, M Alioto "Optimization and evaluation of tapered-VTH approach for energy-efficient CMOS buffers", Proc. of the 20th European Conference on Circuit Theory and Design (ECCTD), Linkoping, Svezia, 2011, pp. 592-595.

[70]. Lanuzza M., Perri S., **Frustaci F**., Corsonello P. “Impact of Process Variations on Flip-Flops Energy and Timing Characteristics” Proc. of IEEE ISVLSI 2010, Lixouri, Kefalonia, Greece, pp. 2010.

[71]. Solanki S., **Frustaci F**., Corsonello P. “A Low-Leakage Single-Ended 6T SRAM Cell” Proc of IEEE ICETET 2010, Bombay, India, 2010.

[72]. De Rose R., **Frustaci F**, Lanuzza M. “Design and Evaluation of High-Speed Energy-Aware Carry Skip Adders” Proc. IEEE ICM 2010, Cairo, Egypt, 2010, pp. 124-127.

[73]. Lanuzza M. , Zicari P. , **Frustaci F**. , Perri S. , Corsonello P. “A Self-Hosting Configuration Management System to Mitigate the Impact of Radiation-Induced Multi-Bit Upsets in SRAM-Based FPGAs” Proc. of IEEE ISIE 2010, Bari, Italy, 2010, pp. 1989-1994.

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Paper awards:

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2021: Silver Leaf Certificate (top 20%) by the technical program committee of the IEEE PRIME 2021 Conference, for the paper:
Salvatore Scarfone, Fabio Frustaci, Stefania Perri "Design and Analysis of a Leading One Detectorbased Approximate Multiplier on FPGA"
In Proceedings of the 16th IEEE Conference on Ph.D. Research in MicroElectronics and Electronics (PRIME'21), online, 2-5 July 2021, pp. 1-4.

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