Stefania Perri – Associate Professor of Electronics

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Stefania Perri was born in Cosenza, Italy, on April 6, 1971. She received the Master degree in Computer Science Engineering from the University of Calabria, Arcavacata di Rende, Italy, in 1996, and the PhD in Electronics Engineering from the University Mediterranea of Reggio Calabria, in 2000. In 2000 she joined the Department of Electronics, Computer Science and Systems of the University of Calabria, Italy, and started her academic career as a post-doc researcher. In 2002, she was appointed as an Assistant Professor, and then in 2010 as an Associate Professor.
From 2005 to 2009, Stefania Perri joined the University of Rochester, NY, USA as an Adjunct Assistant Professor.
In 2017, she joined the Department of Mechanical, Energy and Management Engineering (DIMEG) of the University of Calabria, Italy. In 2017, she received the "*Abilitazione*" to Full Professor position from Italian Minister of University and Research. In 2021, she was appointed as vice-Chair of the Ph.D. Program in "INFORMATION AND COMMUNICATION TECHNOLOGIES" at the University of Calabria. Since March 2021, she serves as an Expert Member of the panel "Electronics and Telecommunications" of the Research Foundation - Flanders (FWO). Since January 2024 she is a member of High Performance Edge And Cloud computing (HiPEAC) network.
Her Academic work and teaching experiences are summarized in the following.

Academic Work and teaching Experiences	
2010 – present	Associate Professor of Electronics, University of Calabria, Italy
2002 -2010	Assistant Professor of Electronics, University of Calabria, Italy
2005-2009	Adjunct Assistant Professor, University of Rochester, NY, USA
2000-2002	Post-doc researcher, University of Calabria, Italy
1997-2000	PhD student, University of Reggio Calabria, Italy
1997	Lecturer of the Master Degree course *Digital Electronics Systems*, University of Reggio Calabria, Italy
1997-2003	Teaching Assistant for the course *Digital Electronics Systems*, University of Calabria, Italy;
1998-2001	Teaching Assistant for the course *Electronics Devices*, University of Reggio Calabria, Italy
2004-2009	Lecturer for the Master Degree courses: *Design of VLSI circuits* and *Electronics for Vision systems*, University of Calabria, Italy
2010-2016	Lecturer for the Bachelor Degree courses: *Digital Electronics* and *Digital Electronics II*, University of Calabria, Italy
2017-present	Lecturer for the Bachelor Degree course *Digital Electronics* and the Master Degree course *Digital Systems Design* and *High-Level Synthesis of Digital Systems* University of Calabria, Italy
2019-present	Lecturer for the Master Degree course *Electronics for IoT Devices* and the level Master post-graduate course *IoT Systems Implementation Hardware level*, University of Calabria, Italy

Her current main research interests include: hardware accelerators for artificial neural networks; reconfigurable systems; approximate computing; design of heterogeneous digital systems; design of QCA

architectures; VLSI and FPGA-based architectures for image processing; low-power designs; hardware security.

Past scientific interests include: VLSI implementation of low-power high-performance arithmetic circuits, asynchronous circuits for arithmetic operations, image compression architectures and low-power multimedia processors.

She has coauthored over 170 technical papers and holds three patents in these fields. She serves on technical committees of several VLSI conferences and as a peer reviewer for several VLSI journals. She is in the Editorial Boards of the *Sensors* journal and the *Journal of Low Power Electronics and Applications*. In 2018 she served as the Guest Editor for the *Journal of Low Power Electronics and Applications* for the special issue on *"Quantum-Dot Cellular Automata (QCA) and Low Power Application"*. Since 2019, she is member of the Program Committee of the "*International Conference on Deep Learning Theory and Applications*" (DeLTA). Since 2023, she is member of the Technical Program Committee of the "International Conference on Design, Automation and Test in Europe" DATE. Since the early 2024 is an Associate Editor of the *Journal of Low Power Electronics and Applications.*

Editorial Activities

- Since 2017, member of the Editorial Board of the "Journal of Low-power Electronics and Applications" (ISSN2079-9268)
- Since 2020, member of the Editorial Board of the journal "Sensors" (ISSN: 1424-8220).
- Guest Editor: 2018 - Journal of Low-power Electronics and Applications (ISSN2079-9268).
- Since 2019, member of the Program Committee of the "International Conference on Deep Learning Theory and Applications" (DeLTA).
- Since 2023, member of the Technical Program Committee of the "International Conference on Design, Automation and Test in Europe" DATE.
- Since the early 2024 is an Associate Editor of the Journal of Low Power Electronics and Applications.

Reviewing for Journals

- IEEE Transactions on Image Processing;
- IEEE Transactions on Circuits and Systems for Video Technology
- IEEE Transactions on Nanotechnology
- IEEE Transactions on VLSI Systems
- IEEE Transactions on Circuits and Systems I
- IEEE Transactions on Circuits and Systems II
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
- IET Circuits, Devices & Systems
- IEE Proceedings on Circuits, Devices & Systems
- IEE Electronics Letters
- Microprocessors and Microsystems Journal
- Journal of Real-Time Image Processing
- International Journal of Circuit Theory and Applications
- Journal of Systems Architecture
- International Journal of Electronics
- Journal of Recent Patents on Signal Processing
- Springer Nature
- Applied Science
- Sensors
- Electronics
- Algorithms
- Journal of Low-Power Electronics and Application
- Journal of Imaging

Technical Program or Reviewing Committee

- International Conference on Design, Automation and Test in Europe" DATE.
- IEEE International conference on Design, Test & Technology of Integrated Systems (DTTIS)
- IEEE International Conference on PhD Research in Microelectronics and Electronics (PRIME)
- International Conference on Deep Learning Theory and Applications (Delta)
- IEEE International Symposium on Circuits and Systems (ISCAS)
- IEEE International Conference on Computer Design (ICCD)
- IEEE International Conference on Electronics, Circuits and Systems (ICECS)
- International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS)
- European conference on circuit theory and design (ECCTD)
- Defect and Fault Tolerance Symposium (DFT)
- International Conference on Field-programmable Logic and Applications (FPL)

Public Funded Grants

- "WEBS-Wireless integrated system for energy, wealth, and security management", Funded by Italian Minister of Economic Development (MISE), 2010-2013.
- "Integrated system for early warning monitoring in case of landslides on highway", Funded by Italian Minister of University and Research (MIUR), 2011-2015
- "Wavelet compressor for real-time high-resolution imaging", Funded by Italian Minister of University and Research (MIUR), 2002-2006
- "High-efficiency photovoltaic systems with specialized diagnostic electronics", Funded by Italian Minister of Economic Development (MISE), 2009-2013
- "MODERN: MOdeling and DEsign of Reliable, process variation-aware Nanoelectronic devices, circuits and systems" Funded by Italian Minister of University and Research (MIUR),2009-2013
- "ERG: Energy for a Green Society: from sustainable harvesting to smart distribution. Equipments, materials, design solutions and their applications", Funded by European Cooperative Program, JTI ENIAC, 2012-2015
- "SMILE – Strumenti e Metodi Intelligenti per la DigitaL Enterprise" Funded by Italian Minister of Economic Development (MISE), 2021-2024
- "R-WINE (RFID - Tracking Wine) Wine Indentification Network Engineering" Funded by POR Calabria FESR 2014/2020
- "E2SG - Energy to Smart Grid" Funded by European Cooperative Program, JTI ENIAC, 2012-2015
- "PICO–e–PRO - Processi Integrati e COnnessi per l'Evoluzione Industriale nella PROduzione" Funded by PON "R&I" 2014-2020
- "Realizzazione in tecnologia VLSI di unità di calcolo riconfigurabili ad alto parallelismo per processori multimediali", Funded by University of Calabria 2003.

Journal Papers

[A90] C. Ieracitano, N. Mammone, F. Spagnolo, F. Frustaci, S. Perri, P. Corsonello, F. C. Morabito, "An explainable embedded neural system for on-board ship detection from optical satellite imagery", Engineering Applications of Artificial Intelligence, Vol. 133, Part E, July 2024.

[A89] F. Spagnolo, S. Perri, M. Vatalaro, F. Frustaci, F. Crupi, P. Corsonello, "Exploring the Usage of Fast Carry Chains to Implement Multistage Ring Oscillators on FPGAs: Design and Characterization", Early paper, IEEE Trans. on VLSI Systems.

[A88] F. Spagnolo, P. Corsonello, F. Frustaci, S. Perri, "Efficient Addition Circuits Using Three-Gate Reconfigurable Field Effect Transistors", Journal of Low Power Electronics and Applications, Vol. 14, n°24, 2024.

[A87] F. Spagnolo, P. Corsonello, F. Frustaci, S. Perri, "Approximate bilateral filters for real-time and low-energyimaging applications on FPGAs", The Journal of Supercomputing, in press.

[A86] F. Spagnolo, P. Corsonello, F. Frustaci, S. Perri, "Efficient implementation of signed multipliers on FPGAs", Computers and Electrical Engineering, Vol. 116, 2024.

[A85] C. Sestito, S. Perri, R. Stewart, “FPGA Design of Transposed Convolutions for Deep Learning Using High-Level Synthesis”, Journal of Signal Processing Systems, vol. 95, n°8, 2023

[A84] F. Spagnolo, P. Corsonello, F. Frustaci, S. Perri, “Design of a Low-power Super-Resolution Architecture for Virtual Reality Wearable Devices”, IEEE Sensors Journal, Vol. 23, n°8, 2023.

[A83] B. Totino, F. Spagnolo, S. Perri, “RIAWELC: A Novel Dataset of Radiographic Images for Automatic Weld Defects Classification”, JOURNAL OF ELECTRICAL AND COMPUTER ENGINEERING RESEARCH, VOL. 3, NO. 1, 2023.

[A82] F. Spagnolo, P. Corsonello, F. Frustaci, S. Perri, "Design of Approximate Bilateral Filters for Image Denoising on FPGAs," IEEE Access, vol. 11, 2023

[A81] S. Perri, F. Spagnolo, F. Frustaci, P. Corsonello, “Welding defects classification through a Convolutional Neural Network”, Manufacturing Letters, vol. 35, 2023

[A80] S. Perri, F. Spagnolo, F. Frustaci, P. Corsonello, “Design of Leading Zero Counters on FPGAs”, IEEE Embedded Systems Letters, Early paper

[A79] F. Frustaci, F. Spagnolo, S. Perri, P. Corsonello; “A High-Speed FPGA-based True Random Number Generator using Metastability with Clock Managers”, IEEE Trans. on Circuits and Systems II: Express Briefs, Vol. 70, n°2, 2023

[A78] S. Perri, F. Spagnolo, F. Frustaci, P. Corsonello; “Designing Energy-Efficient Approximate Multipliers”, Journal of Low Power Electronics and Applications, Vol. 12, n° 4, 2022

[A77] S. Perri, F. Spagnolo, F. Frustaci, P. Corsonello; “Multi-Bit Full Comparator Logic in Quantum-Dot Cellular Automata”, IEEE Trans. on Circuits and Systems II: Express Briefs, vol. 69, no. 11, 2022

[A76] F. Frustaci, F. Spagnolo, S. Perri, G. Cocorullo, P. Corsonello; “Robust and High-Performance Machine Vision System for Automatic Quality Inspection in Assembly Processes”, Sensors, Vol. 22, n°8, 2022.

[A75] F. Spagnolo, S. Perri, P. Corsonello; “Approximate Down-Sampling Strategy for Power-Constrained Intelligent Systems”, IEEE Access, Vol. 10, 2022.

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[A73] C. Sestito, F. Spagnolo, S. Perri; “Design of Flexible Hardware Accelerators for Image Convolutions and Transposed Convolutions”, Journal of Imaging, Vol. 7, n°10, 2021, Switzerland

[A72] S. Perri, F. Spagnolo, F. Frustaci, P. Corsonello; “Accuracy Improved Low-Energy Multi-bit Approximate Adders in QCA”, IEEE Trans. on Circuits and Systems II, Vol. 68, n°11, USA, 2021

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[A68] F. Frustaci, S. Perri, P. Corsonello, M. Alioto; “Approximate Multipliers with Dynamic Truncation for Energy Reduction via Graceful Quality Degradation”, IEEE Trans. on Circuits and Systems II, Vol. 67, n°12, USA, 2020

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[A66] F. Spagnolo, S. Perri, F. Frustaci, P. Corsonello; “Energy-Efficient Architecture for CNNs Inference on Heterogeneous FPGA”, Journal of Low Power Electronics and Applications, Vol. 10, n°1, 2020, Switzerland

[A65] S. Perri, F. Spagnolo, F. Frustaci, P. Corsonello; “Parallel architecture of power-of-two multipliers for FPGAs”, IET Circuits, Devices & Systems, Vol.14, n°3, 2020, United Kingdom

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[A62] F. Frustaci, S. Perri, P. Corsonello,M. Alioto; “Energy-quality Scalable Adders based on Non-zeroing Bit Truncation”, IEEE Trans. on VLSI Systems, Vol.27, n°4, 2019, USA

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[A60] F. Spagnolo, F. Frustaci, S. Perri, P. Corsonello; "An Efficient Connected Component Labeling Architecture for Embedded Systems", Journal of Low Power Electronics and Applications, Vol. 8, n°1, 2018, Switzerland

[A59] G. Cocorullo, P. Corsonello, F. Frustaci, S. Perri; "Design of Efficient BCD adders in Quantum Dot Cellular Automata", IEEE Trans. on Circuits and Systems II, Vol. 64, n.5, 2017, USA

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[A57] G. Cocorullo, P. Corsonello, F. Frustaci, S. Perri; "An Efficient Hardware-Oriented Stereo Matching Algorithm", Microprocessors and Microsystems, Vol.46, Part A, 2016, The Netherlands

[A56] G. Cocorullo, P. Corsonello, F. Frustaci, S. Perri; "Design of Efficient QCA Multiplexers", International Journal of Circuit Theory and Applications, Vol.44, n.3, 2015, USA

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[A53] M. Lanuzza, P. Corsonello, S. Perri; "Fast and Wide Range Voltage Conversion in Multi-Supply Voltage Designs", IEEE Trans. on VLSI Systems, Vol.23, n.2, 2015, USA

[A52] S. Perri, P. Corsonello, G. Cocorullo; "Design of efficient binary comparators in Quantum-Dot Cellular Automata", IEEE Trans. on Nanotechnology, Vol. 13, n°2, 2014, USA

[A51] P. Corsonello, F. Frustaci, M. Lanuzza, S. Perri; "Over/undershooting effects in accurate buffer delay model for sub-threshold domain", IEEE Trans. on Circuits and Systems I, Vol. 61, n°5, USA, 2014

[A50] S. Perri, P. Corsonello, G. Cocorullo; "Area-delay efficient binary adders in QCA", IEEE Trans. on VLSI Systems, Vol. 22, n°5, 2014, USA

[A49] S. Perri, M.Lanuzza, P. Corsonello; "Design of high-speed low-power parallel-prefix adder trees in nanometer technologies", International Journal of Circuit Theory and Applications, Vol. 42, n°7, 2014, USA

[A48] F. Frustaci, M.Lanuzza, S. Perri, P. Corsonello; "Analyzing noise-robustness of wide fan-in dynamic logic gates under process variations", International Journal of Circuit Theory and Applications, Vol. 42, n°5, 2014, USA

[A47] P. Corsonello, M. Lanuzza, S. Perri; "Gate-level body biasing technique for high-speed sub-threshold CMOS logic gates", International Journal of Circuit Theory and Applications, Vol.42, n.1, 2014, USA

[A46] S. Perri, P. Corsonello, G. Cocorullo; "Adaptive Census transform: A novel hardware-oriented stereovision algorithm", Computer Vision and Image Understanding, Vol. 117, n°1, 2013, The Netherlands

[A45] M. Lanuzza, P. Corsonello, S. Perri; "Low-Power Level Shifter for Multi-Supply Voltage Designs", IEEE Trans. on Circuits and Systems II, Vol. 59, n°12, USA, 2012

[A44] S. Perri, P. Corsonello; "New methodology for the design of efficient binary addition circuits in QCA", IEEE Trans. on Nanotechnology, Vol. 11, n°6, 2012, USA

[A43] M. Lanuzza, R. De Rose, F. Frustaci, S. Perri, P. Corsonello; "Comparative Analysis of Yield Optimized Pulsed Flip-Flops", Microelectronics Reliability, Vol. 52, n°8, 2012, The Netherlands

[A42] P.Zicari, S. Perri, P. Corsonello, G. Cocorullo; "Low-cost FPGA stereovision system for real-time disparity maps calculation", Microprocessors and Microsystems, Vol.36, n°4, 2012, The Netherlands

[A41] F.Frustaci, P. Corsonello, S. Perri; "Analytical Delay Model considering variability effects in subthreshold domain", IEEE Trans. on Circuits and Systems II, Vol. 59, n°3, 2012, USA

[A40] F. Frustaci, S. Perri, M. Lanuzza, P. Corsonello; "Energy-Efficient single clock cycle binary comparator", International Journal of Circuit Theory and Applications, Vol.40, n°3, 2012, USA

[A39] M. Lanuzza, F. Frustaci, S. Perri, P. Corsonello; "Design of Energy Aware Adder Circuits Considering Random Intra-Die Process Variations", Journal of Low Power Electronics and Applications, Special issue: Selected Topics in Low Power Design – From Circuits to Applications, Vol. 1, n°1, 2011, Switzerland

[A38] S. Perri, P. Corsonello; “Fast squarer circuits using 3-bit-scan without overlapping bits”, International Journal of Circuit Theory and Applications, Vol. 39, n°19, 2011, USA

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[A35] F. Frustaci, M. Lanuzza, P. Zicari, S. Perri, P. Corsonello; “Low-Power Split-Path Data-Driven Dynamic Logic (SPD3L)”, IET Circuits, Devices and Systems, Vol.3, n°6, 2009 United Kingdom

[A34] S. Purohit, M. Lanuzza, S. Perri, P. Corsonello, M. Margala; “Design and Evaluation of an Energy-Delay-Area Efficient Datapath for Coarse-Grain Reconfigurable Computing Systems”, Journal of Low Power Electronics, Vol.5, n°3, 2009, USA

[A33] F.Frustaci, M. Lanuzza, P. Zicari, S. Perri, P. Corsonello; “Designing High Speed Adders in Power-Constrained Environments”, IEEE Trans. on Circuits and Systems II, Vol.56, n°2, 2009, USA

[A32] F. Frustaci, P. Corsonello, S. Perri, G. Cocorullo; “High-performance noise-tolerant techniques for CMOS dynamic logic”, IET Circuits, Devices and Systems, Vol.2, n°6, United Kingdom, 2008

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[A30] P. Zicari, E. Sciagura, S. Perri, P. Corsonello; “A programmable Carrier-phase independent symbol timing recovery circuit for QPSK/OQPSK signal”, Microprocessors and Microsystems, Vol.32, n°8, The Netherlands, 2008

[A29] P. Zicari, P. Corsonello, S. Perri, G. Cocorullo; “A Matrix Product Accelerator for Field Programmable Systems on Chip”, Microprocessors and Microsystems, Vol.32, n°2, The Netherlands, 2008

[A28] S. Perri, P. Corsonello; “VLSI implementations of efficient isotropic flexible 2D convolvers”, IET Circuits, Devices and Systems, Vol.1, n°4, United Kingdom, 2007

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[A24] S. Perri, P. Corsonello, G. Cocorullo; “Efficient recursive multiply architecture for FPGAs”, IEE Electronics Letters, Vol. 41, n°24, November 2005

[A23] P. Corsonello, S. Perri, M. Margala; “Efficient addition circuits for modular design of Processors-In-Memory”, IEEE Trans. On Circuits and Systems I, Vol.52, n°8, USA, 2005

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International Conference Papers

[B75] S. Perri, C. Zambelli, D. Ielmini, C. Silvano, “Digital In-Memory Computing to Accelerate DeepLearning Inference on the Edge”, (INVITED PAPER) Reconfigurable Architectures Workshop (RAW), San Francisco, USA, May 2024.

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Book Chapters

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Patents

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Awards

INVITED PAPER:

The paper “Digital In-Memory Computing to Accelerate DeepLearning Inference on the Edge” has been invited for the oral presentation in the Session "Reconfigurable Computing Advances in Europe" of the Reconfigurable Architectures Workshop (RAW 2024).

INVITED PRESENTATION:

Stefania Perri was invited at the International Conference on Field-Programmable Logic and Applications FPL 2023 to present the work “Hardware Accelerators for Deep Learning in High-Performance Applications: An Early Survey of the Flagship2 Project of the Italian National Center on HPC”.

INVITED TALK:

Stefania Perri was invited as an Expert Panelist at the Workshop on Parallel AI and Systems for the Edge PAISE 2024.

THE SILVER LEAF CERTIFICATE

Received for the paper “Design and Analysis of a Leading One Detector-based Approximate Multiplier on FPGA” presented at the IEEE Conference PRIME’21.

THE BRONZE LEAF CERTIFCATE

Received for the paper “Run-Time Adaptive Hardware Accelerator for Convolutional Neural Networks” presented at the IEEE Conference PRIME’21.

THE BEST PAPER AWARD WiCAS

Received for the paper “A High-Performance and Power-Efficient SIMD Convolution Engine for FPGAs” presented at the IEEE Conference ICECS 2020.

THE GOLDEN LEAF CERTIFICATE

Received for the paper “Efficient Architecture for Integral Image Computation on Heterogeneous FPGAs” presented at the IEEE Conference PRIME’19.

THE BEST PAPER AWARD

Received for the paper "Evaluating Heterogeneous Architectures based on Zynq AP SOC for Real-Time Video Processing", presented at the International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS 2017).

THE BEST PAPER AWARD

Received for the paper “Color Invariant Study for Background Subtraction” presented at the International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS 2016.

THE BEST PAPER AWARD

Received for the paper “VLSI Circuits for Accurate Motion Estimationpresented at the International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS 2010).

THE BRONZE LEAF CERTIFICATE
Received for the paper “A new scheme to reduce leakage in deep-submicron cache memories with no extra dynamic consumption” presented at the IEEE Conference PRIME’06.

INVITED PAPER:
The paper "A New Reconfigurable Coarse-Grain Architecture for Multimedia Applications" has been invited for the oral presentation in the Session "Adaptive and Reconfigurable Circuits for Multimedia" of the NASA/ESA Conference on Adaptive Hardware and Systems (AHS-2007).

INVITED PAPER:
The paper “Fast, low-cost adders using carry-strength signals”, has been invited for the oral presentation at the Computer&Business Conference SSGRR 2000, L’Aquila, July 2000.

SELECTED BEST PAPER:
The paper “Design-Space Exploration of Energy-Delay-Area Efficient Coarse-Grain Reconfigurable Datapath” has been selected as one of the best papers presented at the International Conference on VLSI design, New Delhi (India), January 2009.

SELECTED BEST PAPER:
The paper “An Efficient and Low-Cost Design Methodology to Improve SRAM-based FPGA Robustness in Space and Avionics Applications” has been selected as one of the best papers presented at the International Workshop on Applied Reconfigurable Computing: Architectures, Tools and Applications, Karlsrue (Germania), March 2009.